US009472508B2

(12) **United States Patent**
Lin et al.

(10) **Patent No.: US 9,472,508 B2**

(45) **Date of Patent: Oct. 18, 2016**

(54) **INTERCONNECT ARRANGEMENT WITH STRESS-REDUCING STRUCTURE AND METHOD OF FABRICATING THE SAME**

(71) Applicant: **Taiwan Semiconductor Manufacturing Co., Ltd.**, Hsinchu (TW)

(72) Inventors: **Yi-Ruei Lin**, Taipei (TW); **Yen-Ming Peng**, Taoyuan County (TW); **Han-Wei Yang**, Hsinchu (TW); **Chen-Chung Lai**, Hsinchu (TW)

(73) Assignee: **Taiwan Semiconductor Manufacturing Co., Ltd.**, Hsinchu (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **14/987,429**

(22) Filed: **Jan. 4, 2016**

(65) **Prior Publication Data**

US 2016/0118350 A1 Apr. 28, 2016

Related U.S. Application Data

(63) Continuation of application No. 14/162,158, filed on Jan. 23, 2014, now Pat. No. 9,252,047.

(51) **Int. Cl.**

H01L 23/58	(2006.01)
H01L 23/00	(2006.01)
H01L 23/48	(2006.01)
H01L 21/768	(2006.01)
H01L 23/31	(2006.01)
H01L 23/532	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 23/562*** (2013.01); ***H01L 21/76801*** (2013.01); ***H01L 21/76808*** (2013.01); ***H01L 21/76822*** (2013.01); ***H01L 21/76877*** (2013.01); ***H01L 23/3178*** (2013.01); ***H01L 23/481*** (2013.01); ***H01L 23/53295*** (2013.01); *H01L 2924/0002* (2013.01)

(58) **Field of Classification Search**

CPC . H01L 23/481; H01L 23/485; H01L 23/522; H01L 23/528; H01L 23/58; H01L 23/585; H01L 24/11

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

2010/0273319 A1 10/2010 Mikami et al.
2011/0057297 A1* 3/2011 Lee H01L 23/562 257/620
2012/0248581 A1 10/2012 Sugiyama et al.
2013/0270712 A1 10/2013 Chen et al.
2013/0334669 A1 12/2013 Kuo et al.

OTHER PUBLICATIONS

C.-J. Weng, "Novel Approach of Semiconductor Manufacturing Process on Copper Dual Damascene Processes Integration" Jun. 2009. Strain, vol. 45, pp. 221-231.

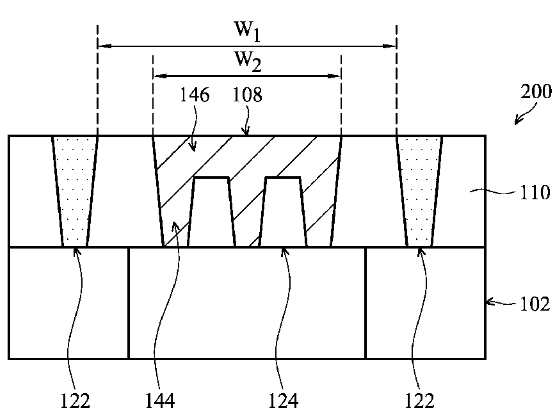
* cited by examiner

Primary Examiner — Kyoung Lee
(74) *Attorney, Agent, or Firm* — Birch, Stewart, Kolasch & Birch, LLP

(57) **ABSTRACT**

A semiconductor device structure and a method of fabricating the same are provided. The semiconductor structure includes a substrate and an interconnection structure formed over the substrate. The interconnection structure includes a first dielectric layer and a first stress-reducing structure formed in the first dielectric layer. The interconnection structure further includes a first conductive feature formed in the first dielectric layer, and the first conductive feature is surrounded by the first stress-reducing structure.

20 Claims, 11 Drawing Sheets



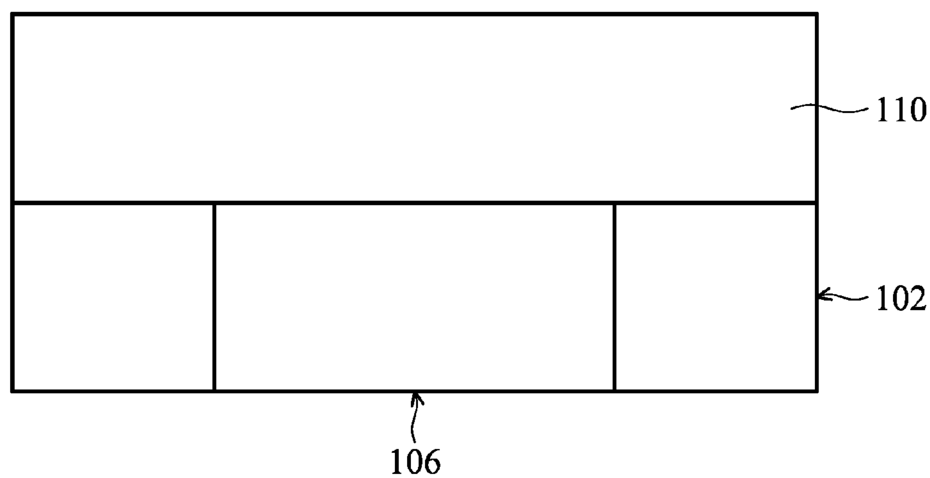


FIG. 1A

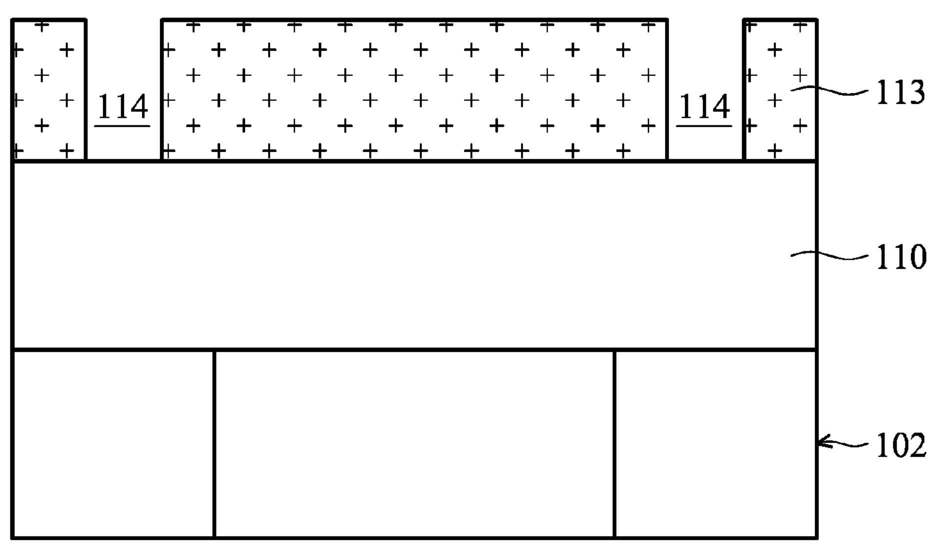


FIG. 1B

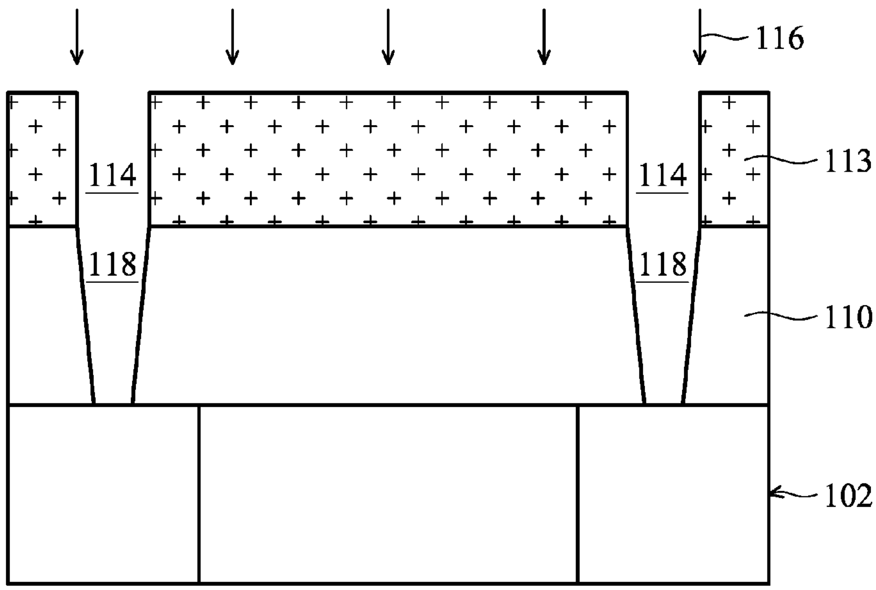


FIG. 1C

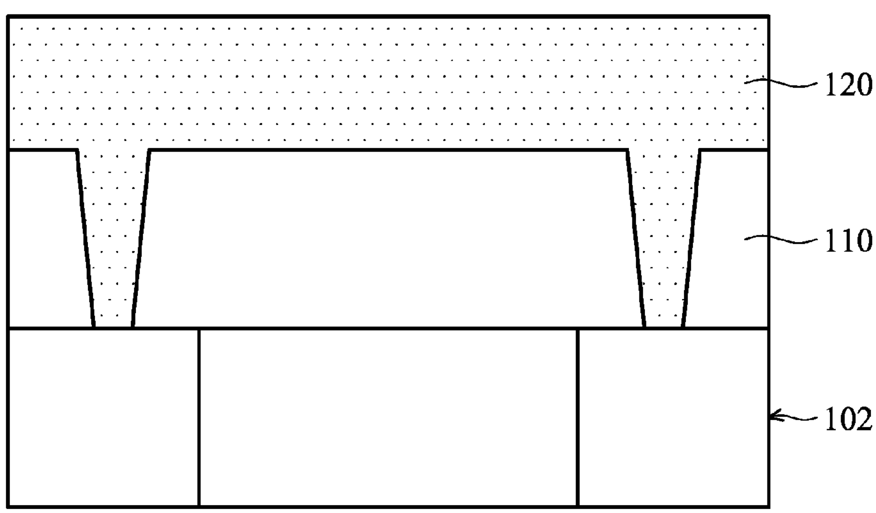


FIG. 1D

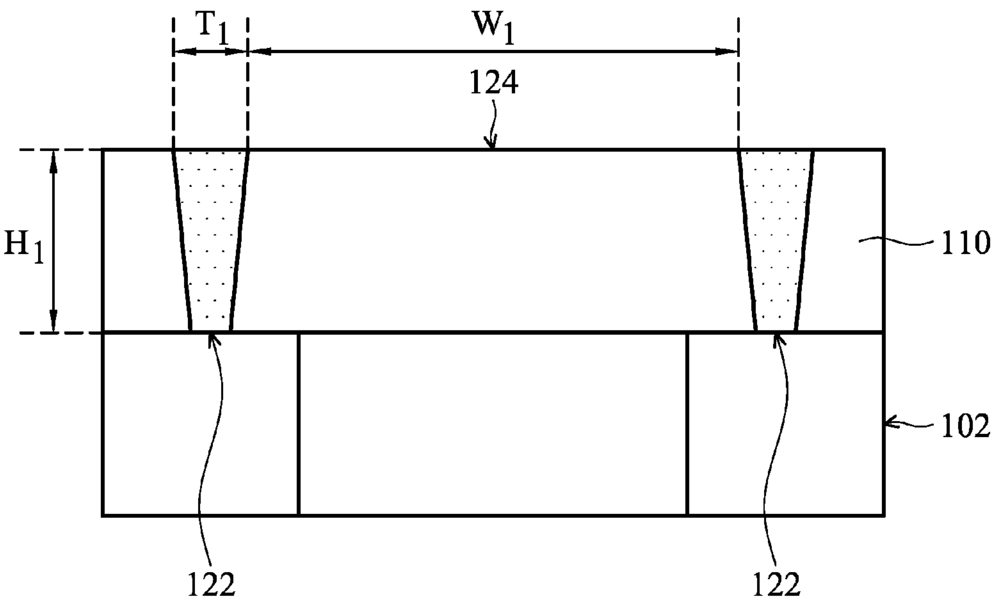


FIG. 1E

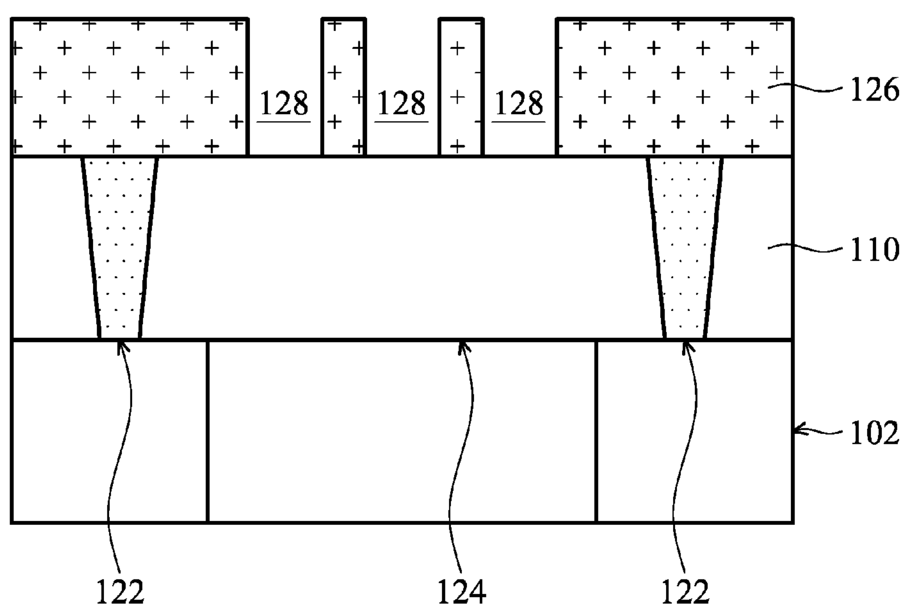
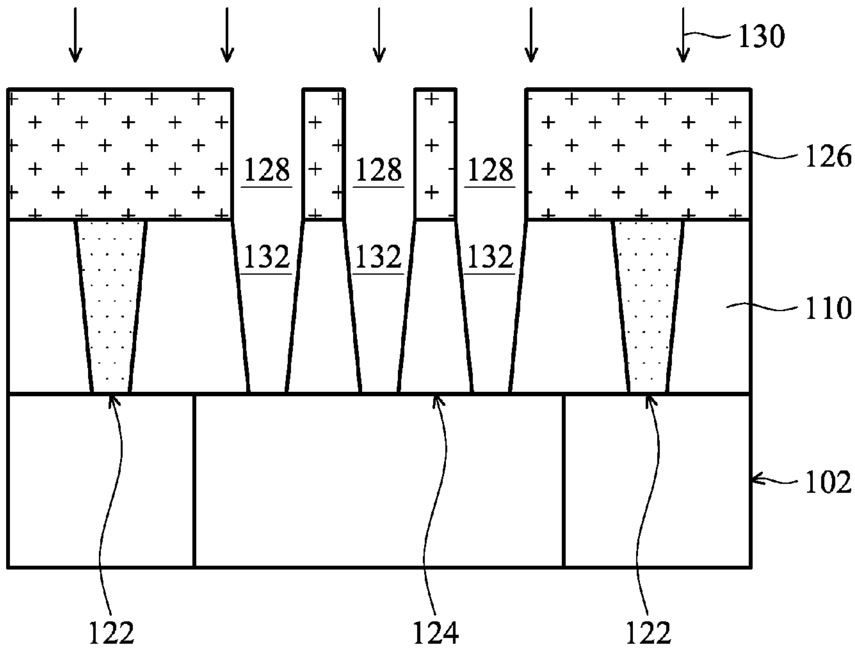
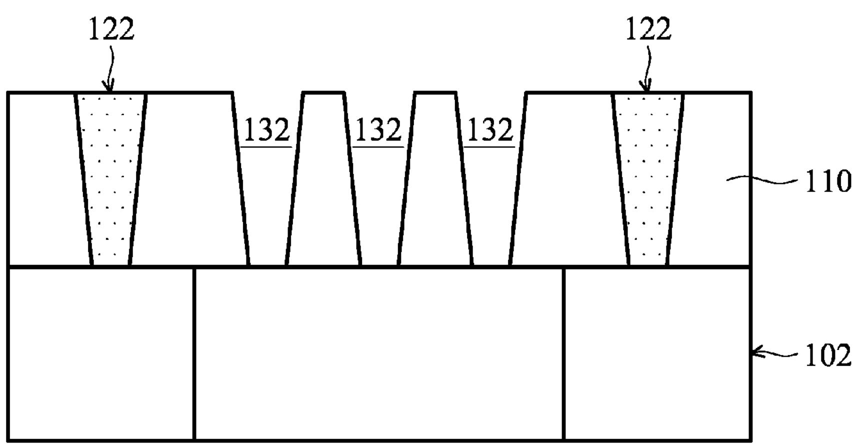


FIG. 1F



130
126
128
128
128
132
132
132
110
102
122
124
122

FIG. 1G



122
122
132
132
132
110
102

FIG. 1H

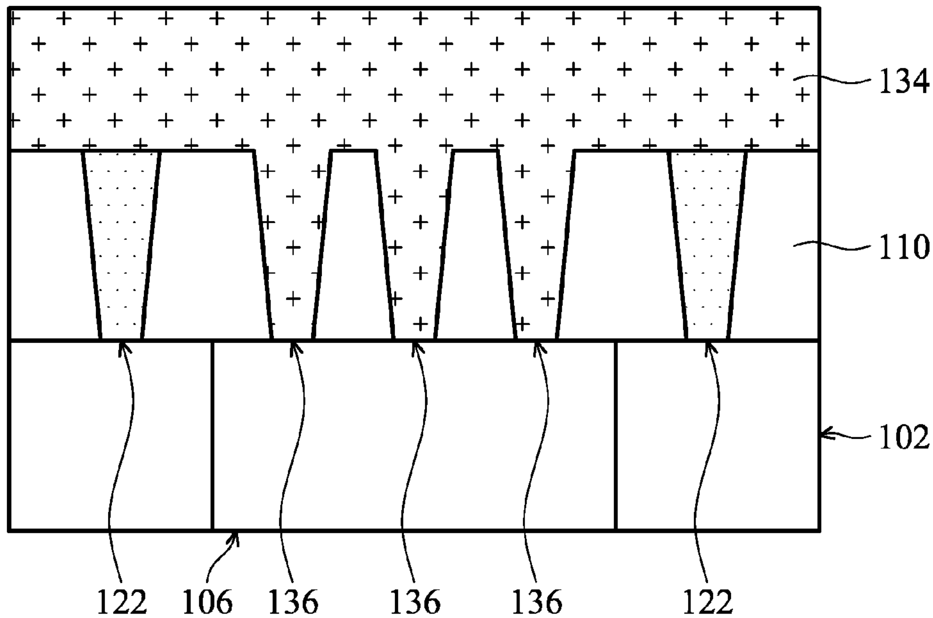

134
110
102
122
106
136
136
136
122

FIG. 1 I

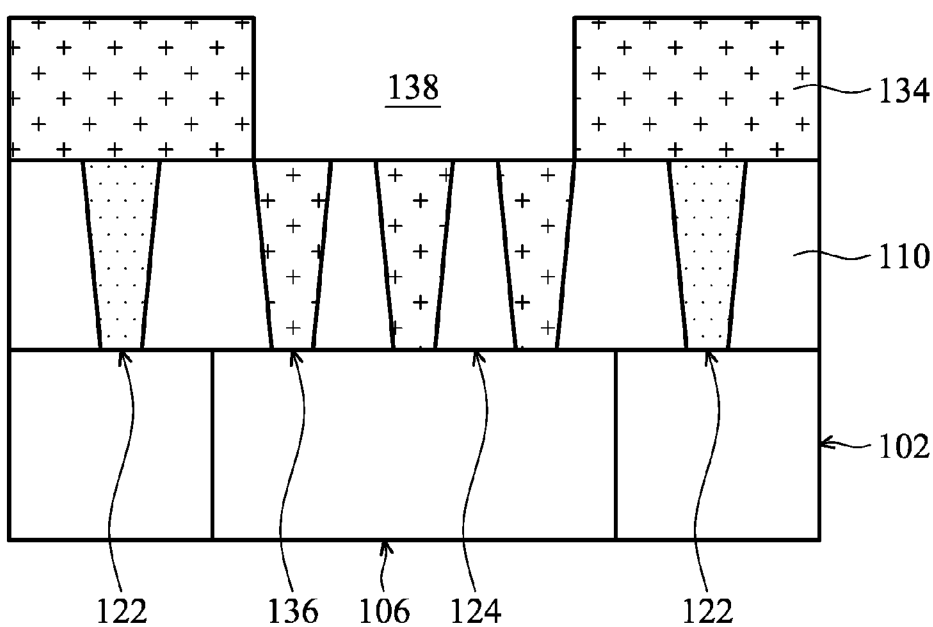

138
134
110
102
122
136
106
124
122

FIG. 1 J

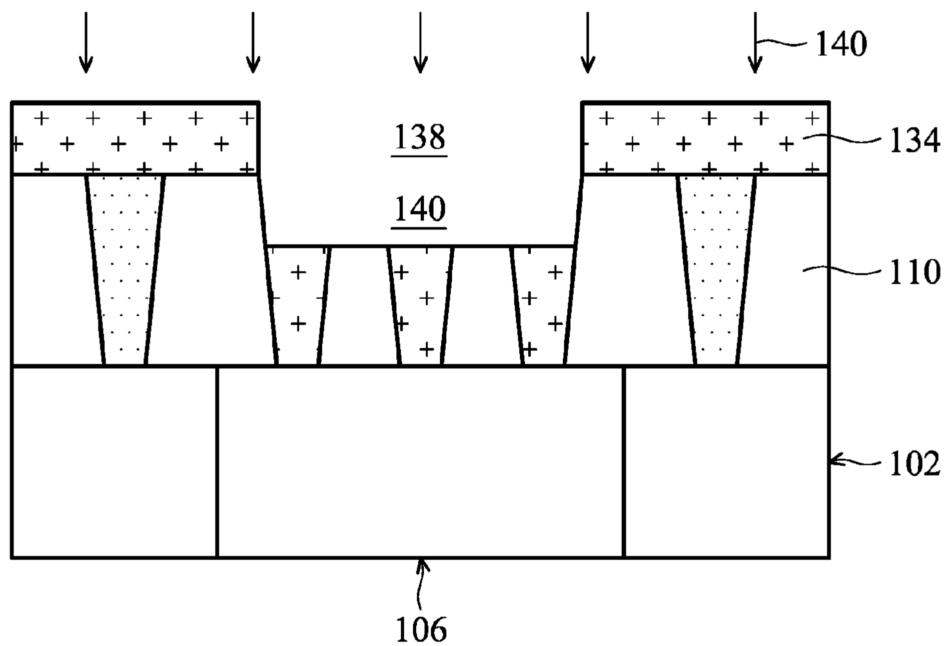


FIG. 1K

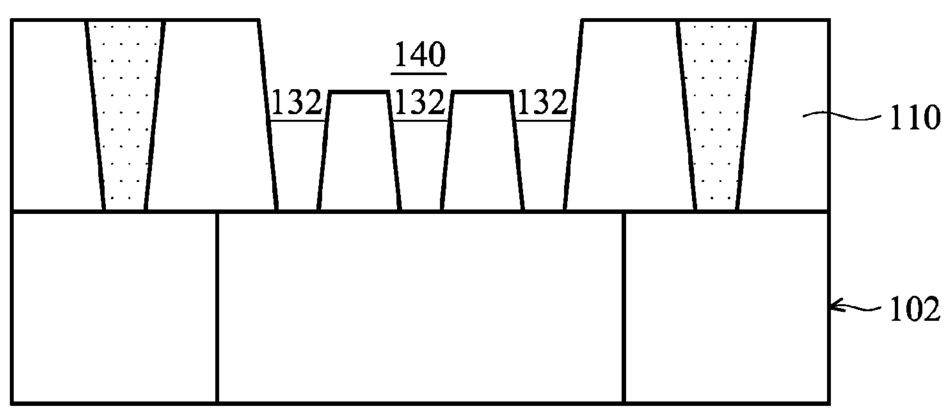


FIG. 1L

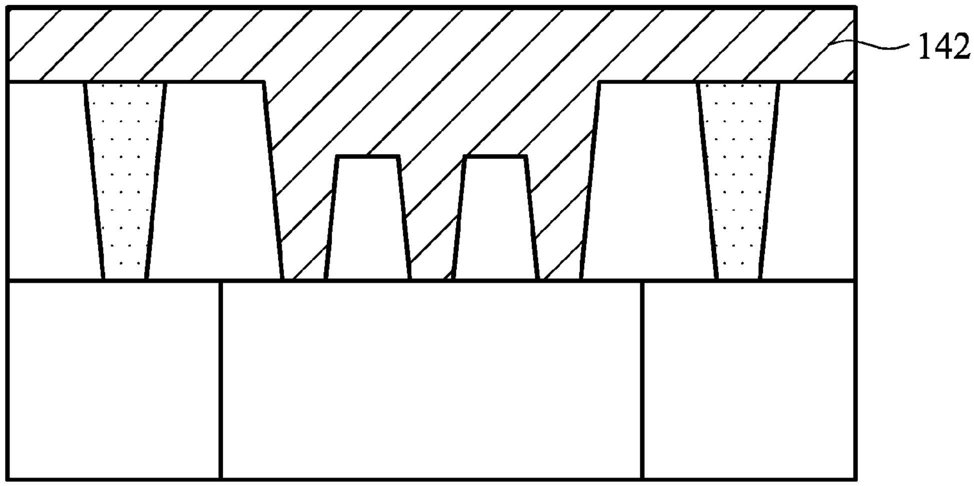


FIG. 1M

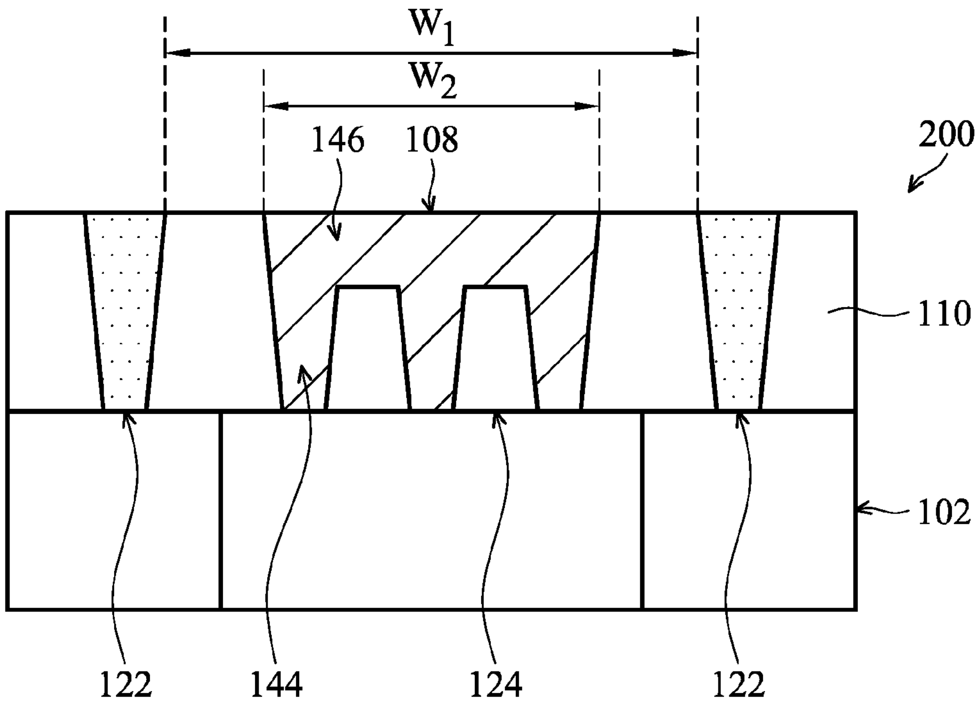


FIG. 1N

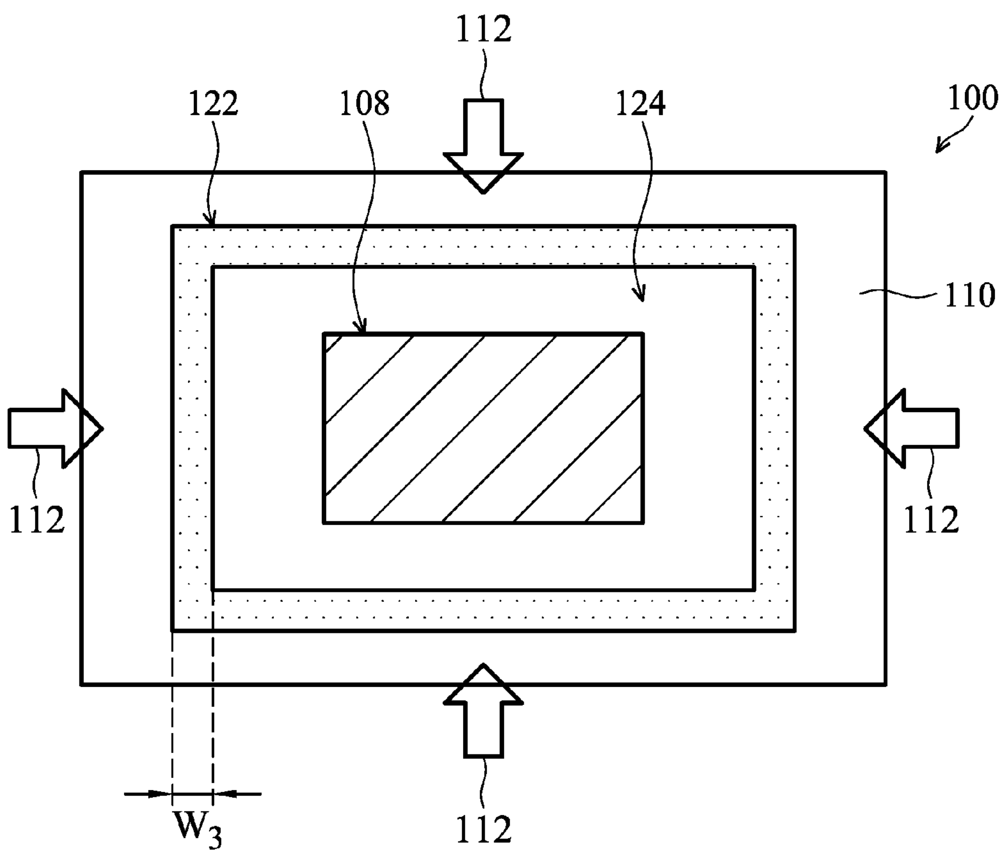


FIG. 2

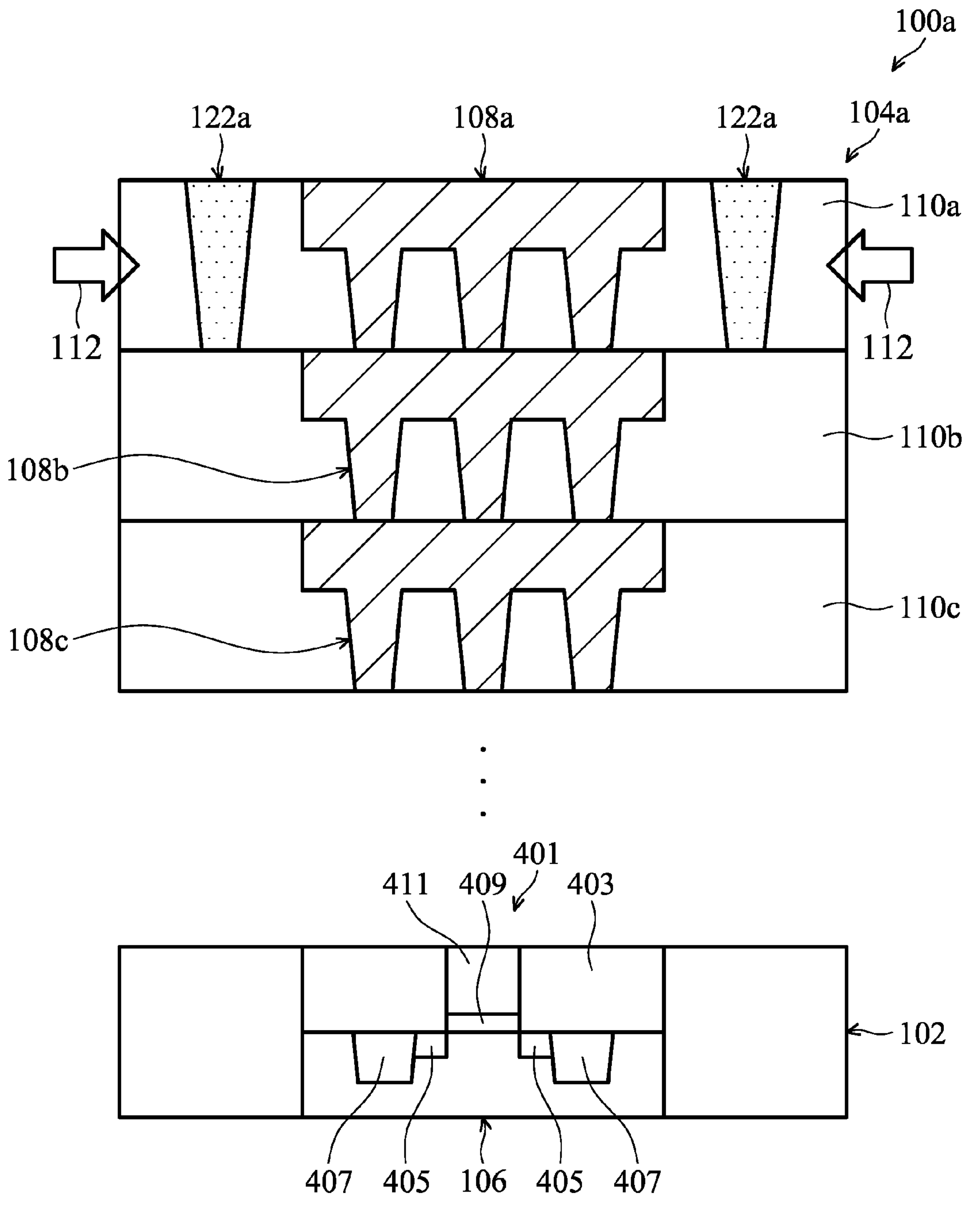

100a
122a
108a
122a
104a
110a
112
112
110b
108b
110c
108c
401
411
409
403
102
407
405
106
405
407

FIG. 3A

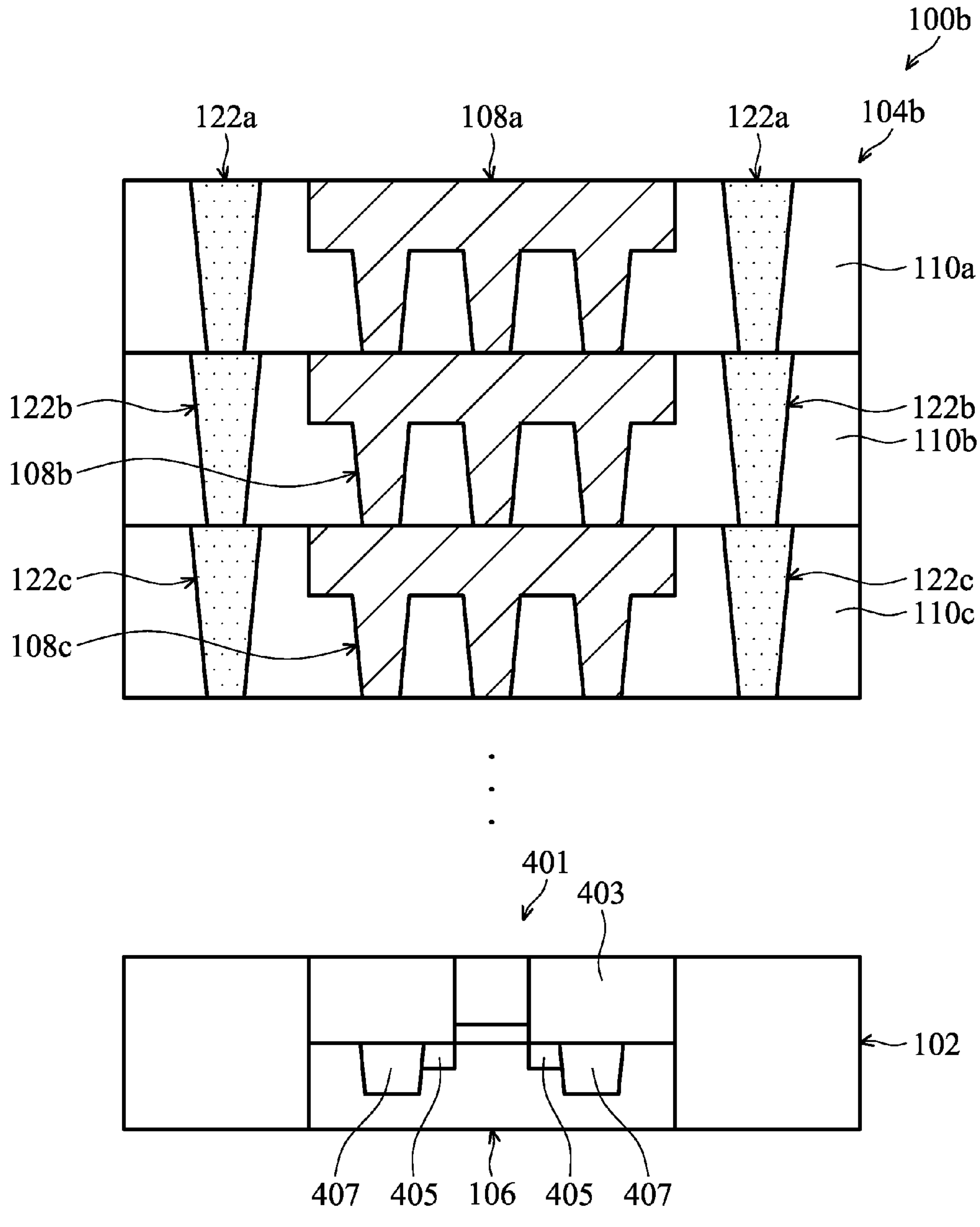

100b
122a
108a
122a
104b
110a
122b
122b
110b
108b
122c
122c
110c
108c
401
403
102
407
405
106
405
407

FIG. 3B

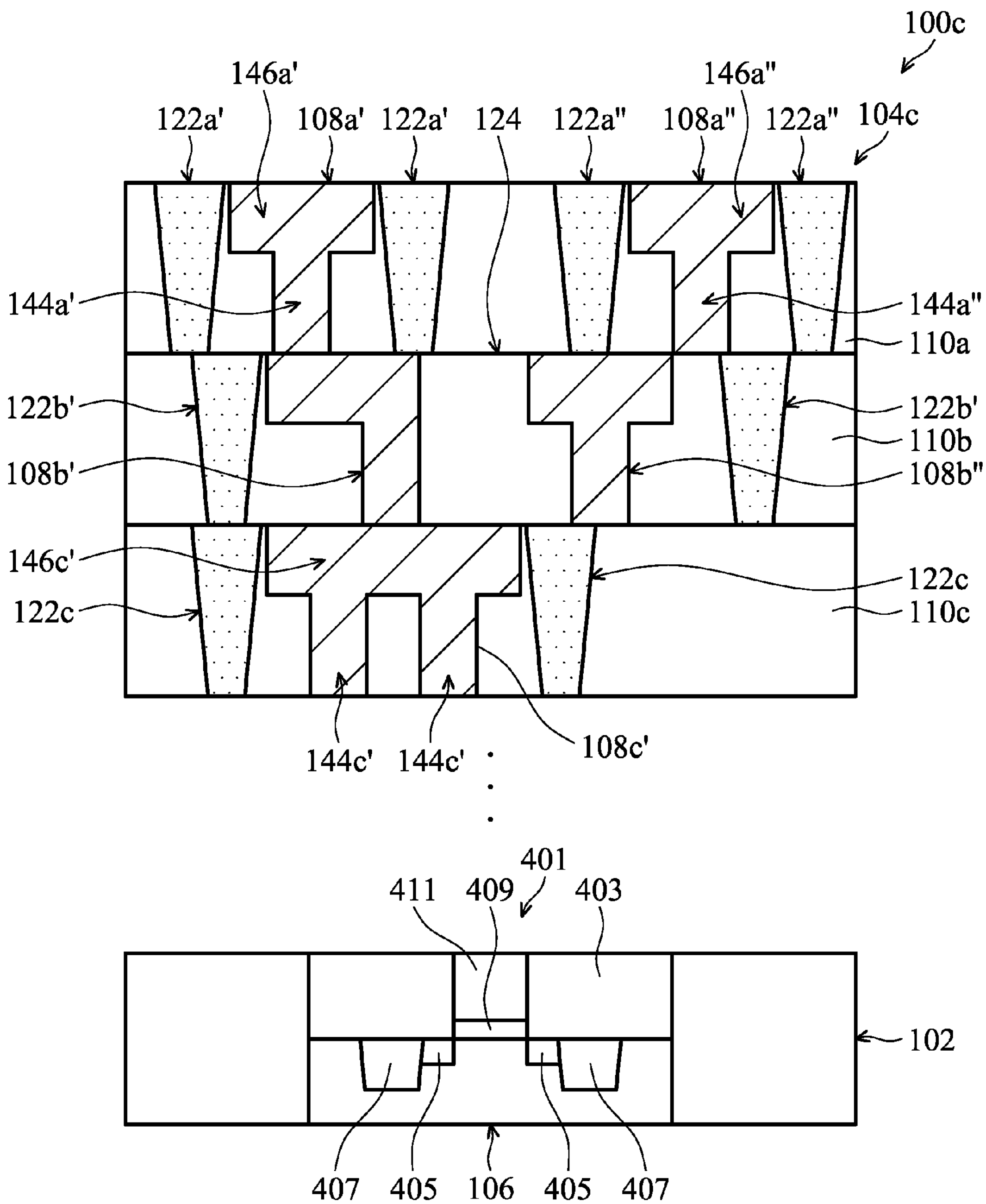

100c
146a'
146a"
122a'
108a'
122a'
124
122a"
108a"
122a"
104c
144a'
144a"
110a
122b'
122b'
110b
108b'
108b"
146c'
122c
122c
110c
144c'
144c'
108c'
401
411
409
403
102
407
405
106
405
407

FIG. 3C

INTERCONNECT ARRANGEMENT WITH STRESS-REDUCING STRUCTURE AND METHOD OF FABRICATING THE SAME

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a Continuation of copending U.S. patent application Ser. No. 14/162,158, filed on Jan. 23, 2014, which is hereby expressly incorporated by reference into the present application herein.

BACKGROUND

Semiconductor devices are used in a variety of electronic applications, such as personal computers, cell phones, digital cameras, and other electronic equipment. Semiconductor devices are typically fabricated by sequentially depositing insulating or dielectric layers, conductive layers, and semiconductive layers of material over a semiconductor substrate, and patterning the various material layers using lithography to form circuit components and elements thereon.

One of the important drivers for increased performance in computers is the higher levels of integration of circuits. This is accomplished by miniaturizing or shrinking device sizes on a given chip. As feature densities in the semiconductor devices increase, the widths of the conductive lines, and the spacing between the conductive lines of back-end of line (BEOL) interconnect structures in the semiconductor devices also need to be scaled down.

However, although existing methods for forming interconnect structures have been generally adequate for their intended purposes, as device scaling-down continues, they have not been entirely satisfactory in all respects.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present disclosure, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIGS. **1A**-**1N** are cross-sectional representations of various stages of forming a semiconductor device structure in accordance with some embodiments.

FIG. **2** is a top-view representation of a semiconductor device structure in accordance with some embodiments.

FIGS. **3A**-**3C** are cross-sectional representations of various semiconductor device structures in accordance with various embodiments.

DETAILED DESCRIPTION

The making and using of various embodiments of the disclosure are discussed in detail below. It should be appreciated, however, that the various embodiments can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative, and do not limit the scope of the disclosure.

It is to be understood that the following disclosure provides many different embodiments, or examples, for implementing different features of the disclosure. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. Moreover, the performance of a first process before a second process in the description that follows may include embodiments in which the second process is performed immediately after the first process, and may also include embodiments in which additional processes may be performed between the first and second processes. Various features may be arbitrarily drawn in different scales for the sake of simplicity and clarity. Furthermore, the formation of a first feature over or on a second feature in the description may include embodiments in which the first and second features are formed in direct or indirect contact.

Some variations of the embodiments are described. Throughout the various views and illustrative embodiments, like reference numbers are used to designate like elements. It is understood that additional operations can be provided before, during, and after the method, and some of the operations described can be replaced or eliminated for other embodiments of the method.

Embodiments of a semiconductor device structure and a method for fabricating the same are provided in accordance with some embodiments of the disclosure. The semiconductor device structure may include an interconnect structure having a conductive feature formed in a dielectric layer.

FIGS. **1A**-**1N** illustrate cross-sectional representations of various stages of forming a semiconductor device structure **100** in accordance with some embodiments. As shown in FIG. **1A**, a substrate **102** is provided in accordance with some embodiments. Substrate **102** may be a semiconductor wafer such as a silicon wafer. Alternatively or additionally, substrate **102** may include elementary semiconductor materials, compound semiconductor materials, and/or alloy semiconductor materials. Examples of the elementary semiconductor materials may be, but are not limited to, crystal silicon, polycrystalline silicon, amorphous silicon, germanium, and/or diamond. Examples of the compound semiconductor materials may be, but are not limited to, silicon carbide, gallium arsenic, gallium phosphide, indium phosphide, indium arsenide, and/or indium antimonide. Examples of the alloy semiconductor materials may be, but are not limited to, SiGe, GaAsP, AlInAs, AlGaAs, GaInAs, GaInP, and/or GaInAsP.

Substrate **102** includes device region **106**, as shown in FIG. **1A** in accordance with some embodiments. Device region **106** may have various device elements. Examples of device elements may include, but are not limited to, transistors, diodes, and/or other applicable elements. Examples of the transistors may include, but are not limited to, metal oxide semiconductor field effect transistors (MOSFET), complementary metal oxide semiconductor (CMOS) transistors, bipolar junction transistors (BJT), high voltage transistors, high frequency transistors, p-channel and/or n-channel field effect transistors (PFETs/NFETs), or the like. Various processes are performed to form the device elements, such as deposition, etching, implantation, photolithography, annealing, and/or other applicable processes. In some embodiments, device region **106** is formed in substrate **102** in a front-end-of-line (FEOL) process.

A dielectric layer **110** is formed over substrate **102**, as shown in FIG. **1A** in accordance with some embodiments. In some embodiments, dielectric layer **110** is an inter-metal dielectric (IMD) layer. Dielectric layer **110** may include multilayers made of multiple dielectric materials, such as a low dielectric constant or an extreme low dielectric constant (ELK) material. Examples of the dielectric materials may include, but are not limited to, oxide, SiO_2, borophosphosilicate glass (BPSG), tetraethyl orthosilicate (TEOS), spin on glass (SOG), undoped silicate glass (USG), fluorinated silicate glass (FSG), high-density plasma (HDP) oxide, or plasma-enhanced TEOS (PETEOS). Dielectric layer **110** may be formed by chemical vapor deposition (CVD), physical vapor deposition, (PVD), atomic layer deposition (ALD), spin-on coating, or other applicable processes.

A first photoresist layer **113** is formed over dielectric layer **110**, and first photoresist layer **113** includes one or more opening **114**, as shown in FIG. **1**B in accordance with some embodiments. The shape of opening **114** may be adjusted as required. In some embodiments, opening **114** has a shape that is an enclosed or non-enclosed circle, rectangle, ellipse, square, or polygon, when viewed from a top view or above (not shown). In some embodiments, opening **114** includes an n-shaped structure, T-shaped structure, bar-shaped structure, and/or a linear structure, when viewed from a top view or above (not shown).

After first photoresist layer **113** is formed, an etching process **116** is performed to etch dielectric layer **110** through opening **114**, as shown in FIG. **1**C in accordance with some embodiments. A stress-reducing structure trench **118** is formed in dielectric layer **110** by etching process **116**. Etching process **116** may be a wet etching process or a dry etching process.

After etching process **116** is performed, first photoresist layer **113** is removed, and a stress-relieving material **120** is provided to fill in stress-reducing structure trench **118**, as shown in FIG. **1**D in accordance with some embodiments. Stress-relieving material **120** is deposited and forms a stress-relieving or stress-reducing guard ring or structure to block or prevent stress forces from acting on the conductive feature formed in sequential processes.

In some embodiment, stress-relieving material **120** is a material different from the material used to form dielectric layer **110**. Therefore, stress-relieving material **120** is capable of stopping stress caused by dielectric layer **110** from reaching conductive feature **108**. In some embodiments, dielectric layer **110** is made of a compressive material such as SiO_2, and stress-relieving material **120** is a tensile material such as Si_3N_4.

In some embodiment, stress-relieving material **120** is silicon oxide, silicon nitride, silicon oxynitride, or a combination thereof. In some embodiment, stress-relieving material **120** is Si_xO_y, and x:y is in a range from about 0.1 to about 10. In some embodiment, stress-relieving material **120** is Si_xN_y, and x:y is in a range from about 0.1 to about 10. In some embodiment, stress-relieving material **120** is $Si_xO_yN_z$, and x:y is in a range from about 0.1 to about 10, or y:z is in a range from about 0.1 to about 10, or x:z is in a range from about 0.1 to about 10. X, y, and z may be adjusted to control the property of stress-relieving material **120**.

Stress-relieving material **120** may be formed or deposited by chemical vapor deposition (CVD), physical vapor deposition (PVD), atomic layer deposition (ALD), high density plasma CVD (HDPCVD), metal organic CVD (MOCVD), plasma enhanced CVD (PECVD), or other applicable deposition processes.

After stress-relieving material **120** fills or is deposited in stress-reducing structure trench **118**, excess portion of stress-relieving material **120** is removed to expose a top surface of dielectric layer **110**, as shown in FIG. **1**E in accordance with some embodiments. The excess portion of stress-relieving material **120** may be removed by a chemical mechanical polishing (CMP) process.

A stress-reducing structure **122** includes stress-reducing structure trench **118**. The shape of stress-reducing structure **122** may be similar to or the same as the shape of opening **114** of first photoresist layer **113**. Although it is not shown in the cross-section representation illustrated in FIG. **1**E, in some embodiments, stress-reducing structure **122** has a shape that is an enclosed or non-enclosed circle, rectangle, ellipse, square, or polygon, when viewed from a top view or above. In some embodiments, stress-reducing structure **122** includes an n-shaped structure, T-shaped structure, bar-shaped structure, and/or a linear structure. It should be noted that stress-reducing structure **122** may include a plurality of portions having the same or different shapes, and some of the portions may intersect with each other, while some of the portions may not intersect with each other.

In some embodiments, stress-reducing structure **122** has a height H_1 in a range from about 0.09 μm to about 35 μm. In some embodiments, stress-reducing structure **122** has a thickness T_1 in a range from about 0.09 μm to about 3 μm.

In addition, as shown in FIG. **1**E, a portion **124** of dielectric layer **110** is surrounded by stress-reducing structure **122** in accordance with some embodiments. Stress-reducing structure **122** is configured to prevent the stress caused or created by dielectric layer **110** from directly entering or acting on portion **124**. Therefore, features formed in portion **124** of dielectric layer **110** are protected by stress-reducing structure **122**. In some embodiments, portion **124** of dielectric layer **110** has a width W_1 in a range from about 0.01 μm to about 50 μm.

After stress-reducing structure **122** is formed, conductive feature **108** is formed in portion **124** of dielectric layer **110** surrounded by stress-reducing structure **122** in accordance with some embodiments. As shown in FIG. **1**F, a second photoresist layer **126** is formed over dielectric layer **110** in accordance with some embodiments. Second photoresist layer **126** includes openings **128** over portion **124** of dielectric layer **110**. It should be noted that although three openings **128** are illustrated in FIG. **1**F, the number of openings **128** in second photoresist layer **126** is not intended to be limiting. For example, second photoresist layer **126** may only include one opening.

Next, an etching process **130** is performed through openings **128**, and via holes **132** are formed in portion **124** of dielectric layer **110**, as shown in FIG. **1**G in accordance with some embodiments. Second photoresist layer **126** is removed after via holes **132** are formed, as shown in FIG. **1**H in accordance with some embodiments.

After second photoresist layer **126** is removed, a third photoresist layer **134** is formed over substrate **102** to cover dielectric layer **110** and stress-reducing structure **122**, as shown in FIG. **1**I in accordance with some embodiments. In addition, portions **136** of third photoresist layer **134** fill in via holes **132**.

Next, an opening **138** is formed in third photoresist layer **134**, as shown in FIG. **1**J in accordance with some embodiments. Opening **138** exposes portions **136** of third photoresist layer **134** formed in via holes **132** and some portions of dielectric layer surrounded (e.g. enclosed) by stress-reducing structure **122**. In some embodiments, opening **138** is formed by an exposure process and a developing process.

After opening **138** of third photoresist layer **134** is formed, an etching process **140** is performed through opening **138** to form a trench **140**, as shown in FIG. **1**K in accordance with some embodiments. More specifically, top portions of portion **136** formed in via holes **132** and top portions of dielectric layer **110** exposed by opening **138** are removed.

After trench **140** is formed, remaining portions of third photoresist layer **134**, including those in via holes **132**, are removed, as shown in FIG. **1**L in accordance with some embodiments. As shown in FIG. **1**L, trench **140** is formed over via holes **132** and is directly connected with via holes **132**.

Next, a conductive material **142** is formed over substrate **102** to fill in trench **140** and via holes **132**, as shown in FIG. **1**M in accordance with some embodiments. Conductive material **142** may be a highly-conductive metal, low-resistive metal, elemental metal, transition metal, or the like. Examples of conductive material **142** may include, but are not limited to, copper (Cu), aluminum (Al), tungsten (W), titanium (Ti), gold (Au), or tantalum (Ta).

After conductive material **142** is formed, a CMP process is performed to form conductive feature **108**, as shown in FIG. **1**N in accordance with some embodiments. In some embodiments, the top surface of stress-reducing structure **122** is substantially level with the top surface of conductive feature **108**. In some embodiments, the top surface of stress-reducing structure **122** is substantially level with the top surface of the conductive feature, and the bottom surface of stress-reducing structure **122** is substantially level with the bottom surface of the conductive feature.

As shown in FIG. **1**N, conductive feature **108**, including vias **144** and a metal line **146**, is formed in portion **124** of dielectric layer **110**. Metal line **146** is formed in trench **140**, and vias **144** in direct contact with metal line **146** are formed in via holes **132**.

In some embodiments, conductive feature **108** has a width W_2 in a range from about 0.01 μm to about 50 μm. Since conductive feature **108** is formed in portion **124** surrounded by stress-reducing structure **122**, width W_2 is less than width W_1.

FIG. **2** illustrates a top view representation of semiconductor device structure **100** in accordance with some embodiments. Conductive feature **108** is formed portion **124** of dielectric layer **110** surrounded (or enclosed) by stress-reducing structure **122**. As shown in FIG. **2**, stress **112** is caused by dielectric layer **110** surrounding conductive feature **108**. In addition, stress **112** may be in a direction toward or away from conductive feature **108**.

More specifically, stress **112** may be a compressive stress or a tensile stress and may be directed toward or imparted on conductive feature **108**. Therefore, if a conductive feature is not surrounded, or protected, by stress-reducing structure **122**, the stress may induce or impart undesired forces on conductive feature **108**. In addition, the forces may result in a change of electron mobility of the device formed in device region **106** under conductive feature **108**. Therefore, the device formed under conductive feature **108** may have poor current uniformity due to stress **112** and the performance of the device may be affected.

Accordingly, conductive feature **108** is formed in portion **124** of dielectric layer **110** surrounded by stress-reducing structure **122**, such that stress **112** cannot reach or do not affect conductive feature **108**, as shown in FIG. **2** in accordance with some embodiments.

In some embodiments, stress-reducing structure **122** shown in a top view has the shape of a rectangle (but is not limited thereto). In some embodiments, stress-reducing structure **122** has a width W_3, and a ratio of the width W_3 to width W_2 is in a range from about 0.01 to about 2.

It should be noted that although embodiments described above, including embodiments illustrated in FIGS. **1**A-**1**N and FIG. **2**, show only one conductive feature formed in one dielectric layer, the semiconductor device structures may include various conductive features in various dielectric layers. That is, the shapes, sizes, and materials of the conductive features may be adjusted depending on their applications, and the scope of the disclosure is not intended to be limiting.

In addition, conductive feature **108** may further include a liner and/or a barrier layer. For example, a liner (not shown) may be formed in trench **140** and via holes **132**, and the liner covers the sidewalls and bottom of trench **140** and via holes **132**. The liner may be either tetraethylorthosilicate (TEOS) or silicon nitride, although any other applicable dielectric may alternatively be used. The liner may be formed using a plasma enhanced chemical vapor deposition (PECVD) process, although other applicable processes, such as physical vapor deposition or a thermal process, may alternatively be used. The barrier layer (not shown) may be formed over the liner (if present) and may cover the sidewalls and bottom of the opening. The barrier layer may be formed using a process such as chemical vapor deposition (CVD), physical vapor deposition (PVD), plasma enhanced CVD (PECVD), plasma enhanced physical vapor deposition (PEPVD), atomic layer deposition (ALD), or any other applicable deposition processes. The barrier layer may be made of tantalum nitride, although other materials, such as tantalum, titanium, titanium nitride, or the like may, also be used.

FIG. **3**A illustrates a cross-sectional representation of a semiconductor device structure **100***a* in accordance with some embodiments. A interconnection structure **104***a* formed in semiconductor device structure **100***a* includes conductive features, such as conductive features **108***a*, **108***b*, and **108***c*. These conductive features are formed in a number of dielectric layers, such as dielectric layers **110***a*, **110***b*, and **110***c*. In addition, conductive feature **108***a* is surrounded by a stress-reducing structure **122***a* formed in dielectric layer **110***a*.

Moreover, device region **106** formed in substrate **102** includes a gate structure **401** embedded in an interlayer dielectric (ILD) layer **403**, source/drain regions **405**, and isolation structures **407**. Since stress-reducing structure **122** is formed to protect conductive feature **108***a* from stress **112**, performance of gate structure **401** can be unaffected although conductive feature **108***a* is formed over gate structure **401**.

In some embodiments, gate structure **401** includes a gate dielectric layer **409**, a gate electrode **411**, and spacers (not shown). In some embodiments, gate dielectric layer **409** is made of high k dielectric materials, such as metal oxides, metal nitrides, metal silicates, transition metaloxides, transition metalnitrides, transition metalsilicates, oxynitrides of metals, or metal aluminates. Examples of the dielectric material may include, but are not limited to, hafnium oxide (HfO_2), hafnium silicon oxide (HfSiO), hafnium silicon oxynitride (HfSiON), hafnium tantalum oxide (HfTaO), hafnium titanium oxide (HfTiO), hafnium zirconium oxide (HfZrO), zirconium silicate, zirconium aluminate, silicon oxide, silicon nitride, silicon oxynitride, zirconium oxide, titanium oxide, aluminum oxide, or hafnium dioxide-alumina (HfO_2—Al_2O_3) alloy.

In some embodiments, gate electrode **411** is made of a conductive material, such as aluminum, copper, tungsten, titanium, tantulum, titanium nitride, tantalum nitride, nickel silicide, cobalt silicide, TaC, TaSiN, TaCN, TiAl, TiAlN, or other applicable materials.

ILD layer **403** may include multilayers made of multiple dielectric materials, such as silicon oxide, silicon nitride, silicon oxynitride, tetraethoxysilane(TEOS), phosphosilicate glass (PSG), borophosphosilicate glass (BPSG), low-k dielectric material, and/or other applicable dielectric materials. Examples of low-k dielectric materials may include, but are not limited to, fluorinated silica glass (FSG), carbon doped silicon oxide, amorphous fluorinated carbon, parylene, bis-benzocyclobutenes (BCB), or polyimide. ILD layer **403** may be formed by chemical vapor deposition (CVD), physical vapor deposition, (PVD), atomic layer deposition (ALD), spin-on coating, or other applicable processes.

It should be noted that device region **106** shown in FIG. **3**A is merely an example, and other devices may be additionally or alternatively formed in device region **106**. In addition, some dielectric layers and conductive features are omitted in FIG. **3**A for clarity.

FIG. **3**B illustrates a cross-sectional representation of a semiconductor device structure **100***b* in accordance with some embodiments. Semiconductor device structure **100***b* is similar to semiconductor device structure **100***a* except stress-reducing structure **122***b* and **122***c* are also formed. More specifically, stress-reducing structure **122***b* is formed in a dielectric layer **110***b* to protect conductive feature **108***b*, and stress-reducing structure **122***c* is formed in a dielectric layer **110***c* to protect conductive feature **108***c*.

FIG. **3**C illustrates a cross-sectional representation of a semiconductor device structure **100***c* in accordance with some embodiments. Semiconductor device structure **100***c* also includes gate structure **401** formed in device region **106** of substrate **102**, similar to that of semiconductor device structure **100***a* or **100***b*.

In addition, conductive features **108***a*' and **108***a*" are formed in dielectric layer **110***a* in accordance with some embodiments. Conductive feature **108***a*' is surrounded by a stress-reducing structure **122***a*', and conductive feature **108***a*" is surrounded by a stress-reducing structure **122***a*". As shown in FIG. **3**C, conductive feature **108***a*' includes one metal line **146***a*' and one via **144***a*' connected with metal line **146***a*'. In addition, conductive feature **108***a*" includes one metal line **146***a*" and one via **144***a*" connected with metal line **146***a*". Moreover, in some embodiments, the edges of conductive feature **108***a*" are in direct contact with stress-reducing structure **122***a*", as shown in FIG. **3**C in accordance with some embodiments.

Furthermore, conductive features **108***b*' and **108***b*" are formed in dielectric layer **110***b*, and conductive feature **108***c*' is formed in dielectric layer **110***c* in accordance with some embodiments. As shown in FIG. **3**C, conductive features **108***b*' and **108***b*" are both formed in portion **124** which is surrounded by a stress-reducing structure **122***b*'. Therefore, conductive features **108***b*' and **108***b*" are both protected by stress-reducing structure **122***b*'. Conductive feature **108***c*' includes one metal line **146***c*' and two vias **144***c*' connected with metal line **146***c*' and is protected by stress-reducing structure **122***c*'.

As shown in FIG. **3**C, conductive features, such as conductive features **108***a*', **108***a*", **108***b*', **108***b*", and **108***c*', with different shapes and sizes can be formed in interconnect structure **104***c*. Accordingly, the application of stress-reducing structure, such as stress-reducing structure **122***a*', **122***a*", **122***b*', and **122***c*, may also be varied, and the scope of the disclosure is not intended to be limiting.

As described previously, when a conductive feature is unprotected, stress caused by dielectric layer surrounding the conductive feature will induce or impart undesired forces, such as pulling forces, on the conductive feature and will affect the performance of devices formed under conductive feature **108**. For example, the electron mobility of the devices may be altered and the devices may have poor current uniformity. Therefore, in various embodiments, the stress-reducing structure, such as stress-reducing structure **122**, is formed to protect the conductive features, such as conductive feature **108**. As shown in FIG. **1**N, conductive feature **108** is formed in portion **124** of dielectric layer **110**. Accordingly, conductive feature **108** is surrounded, and protected, by stress-reducing structure **122**, and the performance of the devices formed in device region **106** under conductive feature **108** is not affected by stress **112**.

Embodiments of mechanisms for a semiconductor device structure are provided. The semiconductor device structure includes a conductive feature formed in a dielectric layer. In addition, the conductive feature is surrounded by a stress-reducing structure (e.g. a guard ring) formed in the dielectric layer. The stress-reducing structure is configured to protect the conductive feature from the stress forces caused by the dielectric layer outside the stress-reducing structure. Therefore, the performance of the devices formed below the conductive feature will not be affected by the stress forces.

In some embodiments, a semiconductor structure is provided. The semiconductor structure includes a substrate and an interconnection structure formed over the substrate. The interconnection structure includes a first dielectric layer and a first stress-reducing structure formed in the first dielectric layer. The interconnection structure further includes a first conductive feature formed in the first dielectric layer, and the first conductive feature is surrounded by the first stress-reducing structure.

In some embodiments, a semiconductor structure is provided. The semiconductor structure includes a first dielectric layer formed over a substrate and a first stress-reducing structure formed in the first dielectric layer. The semiconductor structure further includes a first conductive feature formed in a portion of the first dielectric layer surrounded by the first stress-reducing structure. In addition, the first dielectric layer is made of a compressive material and the stress-reducing structure is made of a tensile material or wherein the first dielectric layer is made of a compressive material and the stress-reducing structure is made of a tensile material.

In some embodiments, a method for forming a semiconductor structure is provided. The method includes forming a dielectric layer over a substrate and forming a trench in the dielectric layer. The method further includes forming a stress-reducing structure in the trench and forming a conductive feature in the dielectric layer. In addition, the conductive feature is surrounded by the stress-reducing structure.

Although embodiments of the present disclosure and their advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the disclosure as defined by the appended claims. For example, it will be readily understood by those skilled in the art that many of the features, functions, processes, and materials described herein may be varied while remaining within the scope of the present disclosure. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present disclosure. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

What is claimed is:

1. A semiconductor structure, comprising:

a substrate;

a device region formed in the substrate;

an interconnection structure formed over the substrate, wherein the interconnection structure comprises:

a first dielectric layer;

a first stress-reducing structure formed in the first dielectric layer; and

a first conductive feature formed in the first dielectric layer, wherein the first conductive feature is surrounded by the first stress-reducing structure,

wherein the first conductive feature is formed over the device region.

2. The semiconductor structure as claimed in claim **1**, wherein the stress-reducing structure has a shape that is an enclosed or non-enclosed circle, rectangle, ellipse, square, or polygon.

3. The semiconductor structure as claimed in claim **1**, wherein the first dielectric layer is made of a compressive material, and the first stress-reducing structure is made of a tensile material.

4. The semiconductor structure as claimed in claim **1**, wherein the first dielectric layer is made of a tensile material, and the first stress-reducing structure is made of a compressive material.

5. The semiconductor structure as claimed in claim **1**, wherein the first stress-reducing structure is made of silicon oxide, silicon nitride, or silicon oxynitride.

6. The semiconductor structure as claimed in claim **1**, wherein the device region includes a gate structure.

7. The semiconductor structure as claimed in claim **1**, further comprising:

a second dielectric layer formed over the first dielectric layer;

a second stress-reducing structure formed in the second dielectric layer; and

a second conductive feature formed in the second dielectric layer, wherein the second conductive feature is surrounded by the second stress-reducing structure.

8. The semiconductor device structure as claimed in claim **1**, wherein a top surface of the first stress-reducing structure is substantially level with a top surface of the first conductive feature, and a bottom surface of the first stress-reducing structure is substantially level with a bottom surface of the first conductive feature.

9. A semiconductor structure, comprising:

a first dielectric layer formed over a substrate;

a first stress-reducing structure formed in the first dielectric layer; and

a first conductive feature formed in a portion of the first dielectric layer surrounded by the first stress-reducing structure,

wherein the first dielectric layer is made of a compressive material and the stress-reducing structure is made of a tensile material or wherein the first dielectric layer is made of a compressive material and the stress-reducing structure is made of a tensile material.

10. The semiconductor structure as claimed in claim **9**, wherein the first stress-reducing structure has a shape that is an enclosed or non-enclosed circle, rectangle, ellipse, square, or polygon.

11. The semiconductor structure as claimed in claim **9**, further comprising:

a second stress-reducing structure formed in the first dielectric layer; and

a second conductive feature formed in a portion of the first dielectric layer surrounded by the second stress-reducing structure.

12. The semiconductor structure as claimed in claim **9**, further comprising:

a second dielectric layer formed over the first dielectric layer;

a third stress-reducing structure formed in the second dielectric layer; and

a third conductive feature formed in a portion of the second dielectric layer surrounded by the third stress-reducing structure.

13. The semiconductor structure as claimed in claim **9**, wherein the first conductive feature comprises a metal line and a via connected to the metal line, and a top surface of the first stress-reducing structure is substantially level with a top surface of the metal line and a bottom surface of the first stress-reducing structure is substantially level with a bottom surface of the via.

14. The semiconductor structure as claimed in claim **9**, further comprising:

a device region formed in the substrate,

wherein the first conductive feature is formed over the device region.

15. A method for forming a semiconductor structure, comprising:

forming a dielectric layer over a substrate;

forming a trench in the dielectric layer;

forming a stress-reducing structure in the trench; and

forming a conductive feature in the dielectric layer, wherein the conductive feature is surrounded by the stress-reducing structure,

wherein the dielectric layer is made of a compressive material and the stress-reducing structure is made of a tensile material or wherein the dielectric layer is made of a compressive material and the stress-reducing structure is made of a tensile material.

16. The method for forming the semiconductor device structure as claimed in claim **15**, wherein forming the stress-reducing structure in the trench further comprises:

depositing a stress-relieving material in the trench and over the dielectric layer; and

removing a portion of the stress-relieving material to expose a top portion of the dielectric layer.

17. The method for forming the semiconductor structure as claimed in claim **15**, wherein the stress-reducing structure trench has a shape that is an enclosed or non-enclosed circle, rectangle, ellipse, square, or polygon.

18. The method for forming the semiconductor structure as claimed in claim **15**, wherein forming the conductive feature further comprises:

forming a via hole in the dielectric layer, wherein the via hole is surrounded by the stress-reducing structure;

forming a trench in the dielectric layer, wherein the trench is connected to the via hole; and

depositing a conductive material in the via hole and in the trench to form the conductive feature.

19. The method for forming the semiconductor structure as claimed in claim **18**, further comprising:

performing a polishing process to remove a portion of the conducive material, such that a top surface of the stress-reducing structure is substantially level with a top surface of the conductive feature.

20. The method for forming the semiconductor structure as claimed in claim **15**, further comprising:

forming a device region in the substrate,
wherein the conductive feature is formed over the device region.

* * * * *